Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte THOMAS J. SWIRBEL,
JOHN K. ARLEDGE,
and
JOAQUIN BARRETO

Appeal No. 2000-0314
Application No. 08/944,192

ON BRIEF

Before HAIRSTON, BARRETT, and LEVY, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 16.

The disclosed invention relates to a multi-layered printed circuit board that has a central core substrate sandwiched between a photoimaged dielectric layer and a non-

photoimageable dielectric layer. A metallization pattern separates each of the dielectric layers from the central core substrate. Vias are formed in the photoimaged dielectric layer by a photoimaging process, and vias are formed in the non-photoimageable dielectric layer by a laser drilling process.

Claims 1 and 15 are illustrative of the claimed invention, and they read as follows:

1. A multi-layer printed circuit board, comprising:

a central core substrate having first and second major opposing surfaces containing first and second respective metallization patterns;

a photoimaged dielectric layer deposited on the first surface and overlying the first metallization pattern, said photoimaged dielectric layer containing a third metallization pattern and photoimaged vias that electrically connect the third metallization pattern to the underlying first metallization pattern; and

a non-photoimageable dielectric layer deposited on the second surface and overlying the second metallization pattern, said non-photoimageable dielectric layer containing a fourth metallization pattern and laser-formed vias that electrically connect the fourth metallization pattern to the underlying second metallization pattern.

15. A multi-layer printed circuit board comprising:

a photoimaged dielectric layer on one side of a cental core substrate and a non-photoimaged dielectric

layer on an opposite side of the central core substrate, the photoimaged dielectric layer containing electrically conductive vias that are formed by a photolithographic process and the non-photoimaged dielectric layer containing electrically conductive vias that are formed by a laser.

The references relied on by the examiner are:

Ohnuki et al. (Ohnuki)	4,668,332	May 26, 1987
Tsukada et al. (Tsukada)	5,451,721	Sep. 19, 1995
Bhatt et al. (Bhatt)	5,487,218	Jan. 30, 1996
Hoshino[1] (published Japanese Kokai Patent Application)	8-8541	Jan. 12, 1996

Claim 15 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hoshino.

Claims 1 through 11, 14 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino and Bhatt.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino and Ohnuki.

Reference is made to the brief (paper number 9) and the answer (paper number 10) for the respective positions of the appellants and the examiner.

[1] A copy of the translation of this reference is attached.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(b) rejection of claim 15, and the 35 U.S.C. § 103(a) rejection of claims 1 through 14 and 16.

Turning first to the anticipation rejection of claim 15, the examiner indicates (answer, page 4) that Hoshino discloses all of the limitations of product claim 15 except for the photolithographic process and the laser process for making the vias[2] in the photoimaged dielectric layer and the non-photoimaged dielectric layer, respectively. According to the examiner (answer, page 4), the "presence of process limitations in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product." When the claimed invention is to a product, it is the patentability of that product that is determined, not the method by which it is made. In re Thorpe, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985). If the

[2] Hoshino indicates (translation, pages 6, 14, 17, 18 and 21) that the vias in the two dielectric layers are formed by chemical means.

record reflects an advantage or unobvious difference between the claimed product and the prior art product, then the product-by-process rationale for rejecting the claim must be withdrawn. In re Marosi, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983). The admitted prior art (specification, page 1, line 23 through page 2, line 1) and Tsukada (column 1, lines 13 through 16 and 59 through 62) provide evidence of differences between vias formed by three different processes. Vias formed by mechanical drilling are larger than vias formed by photolithographic techniques, and vias formed by the latter technique are larger than vias formed by a laser. A decrease in via size results in a corresponding increase in wiring density of the printed circuit board. An additional advantage of the laser technique for forming vias is that a thicker dielectric can be used in the printed circuit board. In view of the noted advantages of laser formed vias over photolithographically formed vias, the product-by-process reasoning advanced by the examiner can not stand. Thus, the
35 U.S.C. § 102(b) rejection of claim 15 is reversed.

In the 35 U.S.C. § 103(a) rejection of claims 1 through

11, 14 and 16, the examiner used the same product-by-process rationale in connection with the teachings of Hoshino. For all of the reasons expressed supra, this rationale can not stand. Even if the teachings of the two references could be properly combined, the combined teachings would still lack a photoimaged dielectric layer overlying the metallization pattern on one side of the core substrate, and a non-photoimageable dielectric layer overlying the metallization pattern on the other side of the core substrate. In Tsukada, a photoimageable dielectric layer 18 is located over the metallization patterns on both sides of the core substrate (Figure 2C). In Hoshino, a non-photoimageable dielectric layer 4a is located over the metallization patterns on both sides of the core substrate (Figure 1). As a result thereof, the 35 U.S.C. § 103(a) rejection of claims 1 through 11, 14 and 16 is reversed.

The 35 U.S.C. § 103(a) rejection of claims 12 and 13 is reversed because the teachings of Bhatt and Ohnuki do not cure the noted shortcomings in the teachings of Tsukada and Hoshino.

DECISION

The decision of the examiner rejecting claim 15 under 35 U.S.C. § 102(b) is reversed, and the decision of the examiner rejecting claims 1 through 14 and 16 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

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MOTOROLA, INC.
INTELLECTUAL PROPERTY DEPARTMENT
8000 WEST SUNRISE BLVD.
FT. LAUDERDALE, FL 33322